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EXAMINER
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MOORE, IAN N

ART UNIT	PAPER NUMBER
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2661

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Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/637,047

Applicant(s)

ZHOU ET AL

Examiner

Ian N Moore

Art Unit

2661

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1,3-14 and 16-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3-14 and 16-24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 5.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

**DETAILED ACTION**

***Response to Amendment***

1. This is in response to amendment filed on February 17, 2004 (paper # 6).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (U.S. 5,610,914) in view of Petersen (U.S. 5,822,321).

**Regarding claim 1**, Yamada '914 discloses a switch (see Fig. 7, NxN shared buffer memory switch) for switching packets from a plurality of sources (see Fig. 7, input ports 11 to N) comprising:

a memory (see Fig. 7, a shared buffer memory 3, and col. 7, line 20-24) in which portion of the packets are stored (see Fig. 5a, routing information path 13; col. 2, line 48-60; note that a shared buffer memory stores "portion" of the ATM cells. When outputting cells to the memory, at the same time, the routing information is also extracted from the cell header and transferred to the shared memory controller 10. Therefore, it is clear that only the "portion" of the cell (i.e. the ATM cell without the routing information) is stored in the memory.); and

a transferring mechanism (Fig. 7, a cell multiplexer 1 with a transmitting functionality) which transfers a predetermined portions of a packet to the to the memory as the predetermined portions are received, (see col. 7, line 24-29; note that a cell multiplexer outputs the multiplexed cells to the memory. Therefore, it is performing a "transferring" function. Also, note that the ATM fixed size cells are received at the input ports and transmitted to the memory. In order to use ATM technology, the user packet must be broken into "portion" in order to fit in fixed size ATM cell format. Due to the nature of fixed ATM cell size (i.e. 53 octets), each ATM cell is the "predetermined portions" of the user packet, and these "predetermined portions" ATM cells are being stored as they are received at the cell multiplexer), and wherein the packet is transferred to the memory (see FIG. 7, cells are transferred to the shared buffer memory 3).

Yamada '914 does not explicitly disclose transferring predetermined portions of the packet as fixed length segments as the fixed length segments are received followed by a single final segment of any length (see Petersen '321 Fig. 5 and col. 3, line 66 to col. 4, line 17; note that a variable size user packet is divided into the fixed segments, except the last segment, then they are placed into the minicells. The last segment can be any size. Each mini cell is then encapsulated by the ATM cell), less than or equal to the length of the fixed length segments (see Petersen '321 FIG. 5, see col. 4, lines 6-25; note that Last segment 504 has 2 octets, which is less than fixed size length of 16 octets segments).

However, this limitation is taught by Petersen '321. Note that Yamada '914 teaches receiving ATM cells at the input ports, and the nature of the ATM cell of being fixed size, which carries segmented user packet. Yamada '914 also teaches how multiple input ports

transferring ATM cells to the shared buffer memory simultaneously. Yamada '914 does not explicitly teaches how to transforms the variable size user packet into ATM cells; however, Petersen '321 teach how to segment the variable size user data into ATM cells by segmenting process. In particular, Petersen '321 teaches segmenting a variable size packet into the fixed length segment(s) as “portions of the packets”, encapsulating those fixed length segment(s) into ATM cells, and then transmitting the ATM cells that contain segments to FIFO storage/memory buffers. In order to conform to ATM standard and utilize ATM network, taught by Petersen '321, each variable size user packet must be segmented. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Yamada '914 as taught by Petersen '321 for the purpose of providing a telecommunication data transfer protocol that effectively utilizes available bandwidth and avoids the problems associated with switching excessively large cells from one ATM stream to another; see Petersen '321 col. 2, line 20-28. The motivation being that by switching fixed pre-load cells, it can overcome the problems associated with the large cells, and the fixed size cell will fit in any predetermine size container (i.e. fixed size ATM cell or fixed size memory array/register).

**Regarding claim 3,** Petersen '321 discloses the transferring mechanism transfers fixed length segments as they are received, as described above in Claim 1.

Yamada '914 discloses the transferring different packets interleaved among each other as they are received to the memory (see Yamada '914 Fig. 5a and col. 2, line 48- 56; note that the cells from each port (i.e. various packets that belong to various ports) are multiplexed

Art Unit: 2661

utilizing time division multiplexing scheme into the memory. Thus, the “interleaving” process is the “time division multiplexing” process.)

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Yamada '914 as taught by Petersen '321 for the same reason stated in Claim 1 above.

3. Claims 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada '914 and Petersen '321, as applied to claims 2-3 above, and further in view of Cisneors (U.S. Patent 5,166,926).

**Regarding claim 4**, Yamada '914 discloses the transferring mechanism includes an aggregator (see Fig. 7, Cell Multiplexer 1) which receives of packets from the plurality of sources (see Fig. 7, Input Ports 11 to N) described above in Claim 1, 2, and 3.

Neither Yamada '914 nor Petersen '321 explicitly discloses the aggregator receives portions of packets (see Cisneros '926 Fig. 5, Self-routing cross-point planes 550s; and col. 19, line 65 to col. 20, line 33 and line-66-68; per Applicant's Fig. 22 and specification, Aggregator belongs to a switch fabric and the striper delivered the portion of the packets to the aggregator. Note that Cisneros '926 Self-routing cross-point plans 550s are the applicant's “switch fabrics”. Each Self-routing cross plan 550 receives parts of the packets from each input module 260 via Individual leads 530s since other parts of packets (i.e. hearers) are being moved to Content Resolution unit.)

However, this limitation is taught by Cisneros '926. Yamada '914's cell multiplexer unit receives parts of the user packet (i.e. ATM cells) from Cisneros '926's input modules.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Yamada '914 and Petersen '321, as taught by Cisneros '926, for the purpose of providing the feature of possessing a small failure group size in the event of a failure of an input or output module; see Cisneros '926 col. 10, line 15-35. The motivation being that by utilizing multi-stage routing switch and routing parts of packets within a switch, it can increase the robustness of a switch and provide a very high degree of fault tolerance.

**Regarding claim 5**, Yamada '914 discloses the memory includes a memory controller (see Fig. 7, Shared buffer memory control 10; noted that the memory 3 and the memory control 10 are being viewed as one combined system.)

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Yamada '914 and Petersen '321, as taught by Cisneros '926, for the same reason stated in Claim 3 above.

**Regarding claim 6**, Yamada '914 discloses the aggregator uses TDM (see Fig. 5A, time division multiplexer data bus 12) to multiplex packets from different sources to the memory controller, and Petersen '321 discloses transmitting segments of packets as described above in Claims 2-5. Thus, Yamada '914's Cell Multiplexer multiplexes various Petersen '321's segments of packets utilizing TDM to the memory control.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Yamada '914 and Petersen '321, as taught by Cisneros '926, for the same reason stated in Claim 3 above.

**Regarding claim 7**, Yamada '914 discloses the aggregator and sources (see Fig. 7. input ports 11) as described above in Claims 1-5.

Petersen '321 discloses placing an identifier with each segment identifying from which source (see Petersen '321 Fig. 5, user packet 501) the segments came from (see Petersen '321 Fig. 7A CID (minicell connection identifier) and col. 6, line 9-20).

Note that Yamada '914 teaches the input ports where each port is consider is a “source”. Petersen '321 teaches utilizing a minicell connection identifier in each segment. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Yamada '914 and Petersen '321, as taught by Cisneros '926, for the same reason stated in Claim 3 above.

**Regarding claim 8**, Petersen '321 discloses identifiers of each segment as describe above in Claim 7. Yamada '914 discloses the memory controller includes per source queues, and stores each cells in a corresponding per source queue (see Yamada '914 Fig. 5 B, a storage within a Shared buffer memory 3, where it stores the cells from the input ports. Note that each section or each shared memory address is a “source queue” since it performs the queuing functionalities of “writing/storing” operation per port basic.) based on the identifier



of the source (see col. 3, line 9-14; note that the cells from each port is stored in the unique address/location (i.e. BBB address of the shared memory), which is in the buffer memory.)

Note that Petersen '321 teaches utilizing a minicell connection identifier in each segment. Yamada '914 teaches that each cell for each input port is stored/queued according to the respective storage in the shared memory storage with a unique address. Petersen '321 cells segments can be stored utilizing Yamada '914 shared memory/storage for each port. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Yamada '914 and Petersen '321, as taught by Cisneros '926, for the same reason stated in Claim 3 above.

4. Claims 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada '914, Petersen '321, and Cisneros '926, as applied to claims 2-8 above, and further in view of Calamvokis '610 (U.S. Patent 5,557,610).

**Regarding claim 9**, the combined system of Yamada '914, Petersen '321, and Cisneros '926 discloses the memory controller and all the segments for a packet are received at a per source queue as described above in Claims 2-8.

Yamada '914 discloses per destination queues (see Yamada '914 Fig. 10A, FIFOs 9, each of which corresponds to the output port; also see col. 8, line 57-63). Petersen '321 discloses that once all segments for a packet are received, all the segments of the packet are changed to a corresponding per destination queue (see Petersen '321 Fig. 12, FIFO-OUT 1208 and Connection table 1207; and col. 8, line 1-9; Petersen '321 teaches the reassembling

Art Unit: 2661

process. Note that once all the segments (i.e. first, middle, and last segment) arrive, SAR fully reassemble the user packet and transmitted to FIFO-OUT.)

Neither Yamada '914, Petersen '321, nor Cisneros '926 explicitly discloses the memory controller (see Calamvkis'610 Fig. 8, memory data bus 67) includes per destination queues (see Calamvkis'610 Fig. 8, Output Shift Register, S.R.OUT 64 and Fig. 9, plurality of S.R.OUT for line outputs N; note that each output shift register in the shared memory is a "destination queue" since it performs the queuing functionalities of "storing/reading/transmitting" operation for each output.), and the packet are changed from a per source queue (see Calamvkis'610 Fig. 8, Input Shift Register, S.R.IN 61 and Fig. 9, plurality of S.R.IN for line inputs N; note that each input shift register in the shared memory is a "source queue" since it performs the queuing functionalities of "receiving/writing/storing" operation for each input.) to a corresponding per destination queue (see Calamvkis'610 col. 10, line 49 to col. 11, line 2; note that the cells from each input are transferred to each output register in parallel manner. Therefore, it is cleared that the cells are transferred from the input to respective output.)

However, this limitation is taught by Calamvkis'610. Yamada '914's teaches input and output FIFO buffers. Petersen '321 teaches reassembling after receiving all segments of a packet then transmits to output FIFO buffer. Calamvkis'610 teaches how input and output registers within a shared memory exchanges cells between input and output ports. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Yamada '914, Petersen '321, Cisneros '926, as taught by Calamvkis'610, for the purpose of designing a switch core which includes circuitry

Art Unit: 2661

enabling the appropriate routing of cells between input and output ports of the switch core, possibly via a common cell-body memory; see Calamvkis'610 col. 2, line 33-38. The motivation being that by designing a common cell-body memory for routing cells between input and output ports, it can decrease routing time and processing delay.

**Regarding claim 10**, the combined system of Yamada '914, Petersen '321, Cisneros '926, and Calamvkis'610 discloses a memory controller storing segments at per source as described above in Claims 2-9.

Moreover, Petersen '321 discloses acceptance criteria for accepting segments (see Petersen '321 Fig. 6, step 608 “threshold” and step 610 “time-out”), and if the segment is not accepted, then all previously received segments associated with the segment not accepted are purged and any segments associated with the segment not accepted that are received after the segment that was not accepted was received, are ignored (see Petersen '321 Fig. 6, Reassembly state 602 for utilizing threshold and time-out for detecting error, and Abort State 603 for discarding the cells after detecting error; also see col. 5, line 1-40; note that during the reassembly process, the reconstruction of the user packet begins only after receiving the last segment. If the last segment is not received during a threshold period, a time-out occurs. Then the process is in the abort mode by halting reassembly process and return to idle mode. At the Idle mode, the process must begin reassembling from the first segment. Thus, all invalid segment segments receive during the abort mode are discarded since the process is now returning back to the idle mode.)

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Yamada '914, Petersen '321, Cisneros '926, as taught by Calamvkis'610, for the same reason stated in Claim 9 above.

**Regarding claim 11**, Yamada '914 disclose a fabric (see Fig. 7, A Shared buffer memory Switch) in which the aggregator (see Fig. 7, Cell Multiplexer) and the memory controller (see Fig. 7, a combined system of Shared Buffer Memory 3 and Controller 10) are disposed, and including a separator (see Fig. 7, Cell Demultiplexer 7) disposed in the fabric connected to the aggregator.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Yamada '914, Petersen '321, Cisneros '926, as taught by Calamvkis'610, for the same reason stated in Claim 9 above.

**Regarding claim 12**, Yamada '914 discloses a fabric has an aggregator receiving portions of packets and a separator receiving of packets as described above in Claims 2-11. Cisneros '926 discloses a port card having a striper (see Cisneros '926 Fig. 5, Input Modules 260), which sends portions of packets to the switch fabric (see Cisneros '926 Fig. 5 Self-routing cross-point planes 550s, and the cells are routed over multi-paths of the multi-stage switch.) and an unstriper (see Cisneros '926 Fig. 5, Output Modules 270), which receives portions of packets from the switch fabric (see Cisneros '926 col. 19, line 65 to col. 20, line 33 and line-66-68).

Note that Yamada '914 teaches a shared buffer memory switch. Cisneros '926 teaches input modules routing the cells over multi-stage cross connect planes to output modules. Thus, Yamada '914's shared memory switch can be used in Cisneros '926's cross connect plane switch.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Yamada '914, Petersen '321, Cisneros '926, as taught by Calamvkis'610, for the same reason stated in Claim 9 above.

**Regarding claim 13**, Yamada '914 discloses the memory controller (see Fig. 5B, Shared buffer memory 2), a shared memory (see Fig. 5B, shared buffer memory 3), and the source queues are part of the shared memory (see Fig. 5B, MMM and NNN and BBB addressed queues). Calamvkis'610 discloses the memory controller includes a shared memory (see Calamvkis'610 Fig. 9, Memory bank of Shared Cell-body memory 73 and N Port Line SR Block 71), and the destination queues (see Calamvkis'610 Fig. 9, S.R.OUT) and the source queues (see Calamvkis'610 Fig. 9, S.R.IN) are part of the shared memory. Note that Yamada '914's memory controller controls the operation of the memory. Calamvkis'610's memory bank includes the switch SR blocks and memory. Therefore, Yamada '914's shared memory can be included in both input and output registers/buffers of Calamvkis'610. Moreover, Yamada '914's shared buffer memory control can be included a shared memory of Calamvkis'610.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Yamada '914, Petersen '321, Cisneros '926, as taught by Calamvkis'610, for the same reason stated in Claim 9 above.

5. Claims 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (U.S. 5,610,914) in view of Petersen (U.S. 5,822,321).

**Regarding claim 14**, Yamada '914 discloses a method for switching packets comprising the steps of

receiving portions of a packet at a transferring mechanism (see Fig. 7, input ports 11 to N, and a cell multiplexer 1 with a transmitting functionality is the “transferring mechanism”; note that the ATM fixed size cells are received at the input ports. Due to the nature of fixed ATM cell size (i.e. 53 octets), each ATM cell is the “portions” of the user packet. In order to use ATM technology, the user packet must be broken into “portion” in order to fit in fixed size ATM cell format.) of a switch (see Fig. 7, NxN shared buffer memory switch; see also col. 7, line 24-29); and

transferring predetermined portions of the packet to a memory of the switch as the predetermined portions are received at the transferring mechanism (see col. 7, line 24-29; note that a cell multiplexer outputs the multiplexed cells to the memory. Therefore, it is performing a “transferring” function. Also, note that the ATM fixed size cells are received at the input ports and transmitted to the memory. In order to use ATM technology, the user packet must be broken into “portion” in order to fit in fixed size ATM cell format. Due to the nature of fixed ATM cell size (i.e. 53 octets), each ATM cell is the “predetermined portions”

of the user packet, and these “predetermined portions” ATM cells are being stored as they are received at the cell multiplexer), and wherein the packet is transferred to the memory (see FIG. 7, cells are transferred to the shared buffer memory 3).

Yamada '914 does not explicitly disclose transferring the predetermined portions as fixed length segments as the fixed length segments are received at the transferring mechanism followed by a single final segment of any length (see Petersen '321 Fig. 5 and col. 3, line 66 to col. 4, line 17; note that a variable size user packet is divided into the fixed segments, except the last segment, then they are placed into the minicells. The last segment can be any size. The ATM cell then encapsulates each mini cell), less than or equal to the length of the fixed length segments (see Petersen '321 FIG. 5, Last segment 504 has 2 octets, which is less than fixed size length of 16 octets segments), less than or equal to the length of the fixed length segments (see Petersen '321 FIG. 5, see col. 4, lines 6-25; note that Last segment 504 has 2 octets, which is less than fixed size length of 16 octets segments).

However, this limitation is taught by Petersen '321. Note that Yamada '914 teaches receiving ATM cells at the input ports, and the nature of the ATM cell of being fixed size, which carries segmented user packet. Yamada '914 also teaches how multiple input ports transferring ATM cells to the shared buffer memory simultaneously. Yamada '914 does not explicitly teaches how to transforms the variable size user packet into ATM cells; however, Petersen '321 teach how to segment the variable size user data into ATM cells by segmenting process. In particular, Petersen '321 teaches segmenting a variable size packet into the fixed length segment(s) as “portions of the packets”, encapsulating those fixed length segment(s) into ATM cells, and then transmitting the ATM cells that contain segments to FIFO

storage/memory buffers. In order to conform to ATM standard and utilize ATM network, taught by Petersen '321, each variable size user packet must be segmented. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Yamada '914 as taught by Petersen '321 for the purpose of providing a telecommunication data transfer protocol that effectively utilizes available bandwidth and avoids the problems associated with switching excessively large cells from one ATM stream to another; see Petersen '321 col. 2, line 20-28. The motivation being that by switching fixed pre-load cells, it can overcome the problems associated with the large cells.

**Regarding claim 16,** Petersen '321 discloses the step of transferring fixed length segments of different packets as they are received, as described above in Claim 14 and 15.

Yamada '914 discloses transferring of different packets as they are received interleaved among each other to the memory (see Yamada '914 Fig. 5a and col. 2, line 48-56; note that the cells from each port (i.e. various packets that belong to various ports) is multiplexed utilizing time division multiplexing scheme into the memory. Thus, the “interleaving” process is the “time division multiplexing” process.)

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Yamada '914 as taught by Petersen '321 for the same reason stated in Claim 14 above.



Art Unit: 2661

6. Claims 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada '914 and Petersen '321, as applied to claims 15-16 above, and further in view of Cisneors (U.S. Patent 5,166,926).

**Regarding claim 17**, Yamada '914 discloses the step of receiving portions of packets from different sources (see Fig. 7, Input Ports 11 to N) at an aggregator (see Fig. 7, Cell Multiplexer 1) disposed in a fabric of the switch (see Fig. 7, Shared buffer memory switch) described above in Claims 15-16.

Neither Yamada '914 nor Petersen '321 explicitly discloses of receiving portions of packets at an aggregator (See Cisneros '926 Fig. 5, Self-routing cross-point planes 550s; and col. 19, line 65 to col. 20, line 33 and line-66-68; per Applicant's Fig. 22 and specification, Aggregator belongs to a switch fabric and striper delivered the portion of the packets to the aggregator. Note that Cisneros '926 Self-routing cross-point plans 550s are the applicant's "switch fabrics". Each Self-routing cross plan 550 receives parts of the packets from each input module 260 via Individual leads 530s since other parts of packets (i.e. hearers) are being moved to Content Resolution unit.)

However, this limitation is taught by Cisneros '926. Yamada '914's cell multiplexer unit receives parts of the user packet (i.e. ATM cells) from Cisneros '926's input modules. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Yamada '914 and Petersen '321, as taught by Cisneros '926, for the purpose of providing the feature of possessing a small failure group size in the event of a failure of an input or output module; see Cisneros '926 col. 10, line 15-35. The motivation being that by utilizing multi-stage routing switch and routing

Art Unit: 2661

parts of packets within a switch, it can increase the robustness of a switch and provide a very high degree of fault tolerance.

**Regarding claim 18**, Yamada '914 discloses the step of multiplexing with the aggregator packets from different sources (see Fig. 5A, time division multiplexer data bus 12) to the memory controller (see Fig. 7, Shared buffer memory control 10; noted that the memory 3 and the memory control 10 is being viewed as one combined system.). Petersen '321 discloses transmitting segments of packets as described above in Claims 15-17. Thus, Yamada '914's Cell Multiplexer multiplexes various Petersen '321's segments of cells to the memory.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Yamada '914 and Petersen '321, as taught by Cisneros '926, for the same reason stated in Claim 17 above.

**Regarding claim 19**, Yamada '914 discloses the step of placing by the aggregator and sources (see Fig. 7, input ports 11) as described above in Claims 15-18.

Petersen '321 discloses placing an identifier with each segment identifying from which source (see Petersen '321 Fig. 5, user packet 501) the segment came from (see Petersen '321 Fig. 7A CID (minicell connection identifier) and col. 6, line 9-20).

Note that Yamada '914 teaches the input ports where each port is consider is a "source". Petersen '321 teaches utilizing a minicell connection identifier in each segment. Therefore, it would have been obvious to one having ordinary skill in the art at the time the

Art Unit: 2661

invention was made to modify the combined system of Yamada '914 and Petersen '321, as taught by Cisneros '926, for the same reason stated in Claim 17 above.

**Regarding claim 20,** Petersen '321 discloses identifiers of each segment as describe above in Claim 19. Yamada '914 discloses storing each cell in a corresponding per source queues of the memory controller (see Fig. 5 B, storage within a Shared buffer memory 3, where it stores the cells from the input ports. Note that each section or each shared memory address is a “source queue” since it performs the queuing functionalities of “writing/storing” operation per port basic. ) based on the identifier of the source (see col. 3, line 9-14; note that the cells from each port is stored in the unique address/location (i.e. BBB address of the shared memory), which is in the buffer memory.)

Note that Petersen '321 teaches utilizing a minicell connection identifier in each segment. Yamada '914 teaches that each cell for each input port is stored/queued according to the respective storage in the shared memory storage with a unique address. Petersen '321 cells segments can be stored utilizing Yamada '914 shared memory/storage for each port. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Yamada '914 and Petersen '321, as taught by Cisneros '926, for the same reason stated in Claim 17 above.

7. Claims 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada '914, Petersen '321, and Cisneros '926, as applied to claims 15-20 above, and further in view of Calamvokis'610 (U.S. Patent 5,557,610).

**Regarding claim 21**, the combined system of Yamada '914, Petersen '321, and Cisneros '926 discloses the memory controller stores the segments for a packet which are received at a per source queue as described above in Claims 15-20.

Yamada '914 discloses per destination queues (see Fig. 10A, FIFOs 9, each of which corresponds to the output port; also see col. 8, line 57-63). Petersen '321 discloses that once all segments for a packet are received, all the segments of the packet are changed to a corresponding per destination queue (see Petersen '321 Fig. 12, FIFO-OUT 1208 and Connection table 1207; and col. 8, line 1-9; Petersen '321 teaches reassembly process. Note that once all the segments (i.e. first, middle, and last segment) arrive, SAR fully reassemble the user packet and transmitted to FIFO-OUT.)

Neither Yamada '914, Petersen '321, nor Cisneros '926 explicitly discloses the step of changing all segments of the packet (see Calamvkis'610 Fig. 8, Input Shift Register, S.R.IN 61 and Fig. 9, plurality of S.R.IN for line inputs N; note that each input shift register in the shared memory is a "source queue" since it performs the queuing functionalities of "receiving/writing/storing" operation for each input.) in the source queue to a corresponding per destination queue (see Calamvkis'610 Fig. 8, Output Shift Register, S.R.OUT 64 and Fig. 9, plurality of S.R.OUT for line outputs N; note that each output shift register in the shared memory is a "destination queue" since it performs the queuing functionalities of "storing/reading/transmitting" operation for each output. Also, see Calamvkis'610 col. 10, line 49 to col. 11, line 2; note that the cells from each input are transferred to each output register in parallel manner. Therefore, it is cleared that the cells are transferred from the input

to respective output.) of the memory controller (see Calamvkis'610 Fig. 8, memory data bus 67).

However, this limitation is taught by Calamvkis'610. Yamada '914's teaches input and output FIFO buffers. Petersen '321 teaches reassembling after receiving all segments of a packet then transmits to output FIFO buffer. Calamvkis'610 teaches how input and output registers within a shared memory exchanges cells between input and output ports. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Yamada '914, Petersen '321, Cisneros '926, as taught by Calamvkis'610, for the purpose of designing a switch core which includes circuitry enabling the appropriate routing of cells between input and output ports of the switch core, possibly via a common cell-body memory; see Calamvkis'610 col. 2, line 33-38. The motivation being that by designing a common cell-body memory for routing cells between input and output ports, it can decrease routing time and processing delay.

**Regarding claim 22**, the combined system of Yamada '914, Petersen '321, Cisneros '926, and Calamvkis'610 discloses a memory controller storing segments at per source as described above in Claims 15-21.

Moreover, Petersen '321 discloses the steps of purging all previously received segments associated with an unaccepted segment that does not meet acceptance criteria for accepting a segment (see Fig. 6, step 608 "threshold" and step 610 "time-out"), and ignoring all segments associated with the unaccepted segment received at the memory controller after the unaccepted segment is received (see Fig. 6, Reassembly state 602 for utilizing threshold

and time-out for detecting error, and Abort State 603 for discarding the cells after detecting error; also see col. 5, line 1-40; note that during the reassembly process, the reconstruction of the user packet begins only after receiving the last segment. If the last segment is not received during a threshold period, a time-out occurs. Then the process is in the abort mode by halting reassembly process and return to idle mode. At the Idle mode, the process must begin reassembling from the first segment. Thus, all invalid segments receive during the abort mode are discarded since the process is now returning back to the Idle mode.).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Yamada '914, Petersen '321, Cisneros '926, as taught by Calamvkis'610, for the same reason stated in Claim 21 above.

**Regarding claim 23,** Yamada '914 discloses the step of receiving portions of packets from different sources at the aggregator (see Fig. 7, Cell Multiplexer) of the transferring mechanism disposed in the fabric (see Fig. 7, a Shared buffer memory Switch) of the switch. Cisneros '926 discloses a striper of a port card (see Fig. 5, Input Modules 260) of the switch (see Fig. 5 Self-routing cross-point planes 550s).

Note that Yamada '914 teaches receiving portions of cells at the cell multiplexer of a shared buffer switch. Cisneros '926 teaches input modules routing the portions of packets over multi-stage cross connect plans to output modules. Therefore, Yamada '914's shared memory switch can be used in Cisneros '926's cross connect plane switch and Cisneros '926's input modules.

Art Unit: 2661

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Yamada '914, Petersen '321, Cisneros '926, as taught by Calamvkis'610, for the same reason stated in Claim 21 above.

**Regarding claim 24**, Yamada '914 discloses the step of sending portions of packets from the memory controller (see Fig. 7, a combined system of Shared Buffer Memory 3 and Controller 10) with a separator of the fabric (see Fig. 7, Cell Demultiplexer 7). Cisneros '926 discloses sending portions of packets (see Cisneros '926 col. 19, line 65 to col. 20, line 33 and line-66-68) from the fabric (see Cisneros '926 Fig. 5 Self-routing cross-point planes 550s) to an unstriper of the port card (see Cisneros '926 Fig. 5, Output Modules 270).

Note that Yamada '914 teaches sending cells from a shared memory to the demultiplexer. Cisneros '926 teaches routing the portions of packets over multi-stage cross connect plans to output modules. Thus, Yamada '914's shared memory switch can be used in Cisneros '926's cross connect plane switch.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Yamada '914, Petersen '321, Cisneros '926, as taught by Calamvkis'610, for the same reason stated in Claim 21 above.

#### ***Notes/Remarks***

8. Objections to the drawings and specification are withdrawn since they are being amended accordingly.

Art Unit: 2661

9. Claim rejections under 35 USC § 112, second paragraph, on claims 10 and 20 are withdrawn since they are being amended accordingly.

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.



Art Unit: 2661

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N Moore whose telephone number is 703-605-1531. The examiner can normally be reached on M-F: 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Vanderpuye can be reached on 703-308-8251. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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**KENNETH VANDERPUYE**  
**PRIMARY EXAMINER**